THE INVENTION CLAIMED IS:

24. A semiconductor memory device comprising:

at least one first wordline comprising P-type silicon or polysilicon and a first nonconductive silicon oxide layer;

at least one second wordline comprising N-type silicon or polysilicon and a second nonconductive silicon layer; and

wherein the first layer is thicker than the second layer.

25. The semiconductor memory device of Claim 24, wherein the first and second spacers are formed using tetraethylorthosilicate/ ozone deposition in a one step process.

26. The semiconductor memory device of Claim 24, wherein at least one of the first wordline or the second wordline form part of a DRAM array.

27. The semiconductor memory device of Claim 24 wherein the DRAM array is part of a system-on-chip.

28. The semiconductor memory device of Claim 24, wherein at least one of the first wordline or the second wordline form part of an SRAM array.

29. The semiconductor memory device of Claim 24 wherein the SRAM array is part of a system-on-chip.

30. A multi-gate semiconductor device comprising:

at least one first P-type gate surrounded by a first nonconductive silicon oxide layer; and

at least one second N-type silicon gate surrounded by a second nonconductive silicon oxide layer;

wherein the first nonconductive spacer is thicker than the second nonconductive layer.

31. The multi-gate semiconductor device of Claim 30, wherein the device is part of a logic circuit.

Redlined Claims

THE INVENTION CLAIMED IS:

24. A semiconductor memory device comprising:

at least one first wordline comprising P-type silicon or polysilicon and a first nonconductive silicon oxide layer;

at least one second wordline comprising N-type silicon or polysilicon and a second nonconductive silicon layer; and

wherein the first layer is thicker than the second layer.

25. The semiconductor memory device of Claim ~~25~~ 24, wherein the first and second spacers are formed using tetraethylorthosilicate/ ozone deposition in a one step process.

26. The semiconductor memory device of Claim ~~25~~ 24, wherein at least one of the first wordline or the second wordline form part of a DRAM array.

27. The semiconductor memory device of Claim ~~25~~ 24 wherein the DRAM array is part of a system-on-chip.

28. The semiconductor memory device of Claim ~~25~~ 24, wherein at least one of the first wordline or the second wordline form part of an SRAM array.

29. The semiconductor memory device of Claim ~~25~~ 24 wherein the SRAM array is part of a system-on-chip.

30. A multi-gate semiconductor device comprising:

at least one first P-type gate surrounded by a first nonconductive silicon oxide layer; and

at least one second N-type silicon gate surrounded by a second nonconductive silicon oxide layer;

wherein the first nonconductive spacer is thicker than the second nonconductive layer.

31. The multi-gate semiconductor device of Claim 30, wherein the device is part of a logic circuit.